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DIGITAL SECURITY SYSTEM USING FPGA

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Abstract: Nowadays, house security system becomes the best solution to overcome house intrusion problem when user is in house or not in house. As we know, there are many types of house security system which are too expensive and difficult to use. For that reason, an effective house security system at low cost is built where user can also program the security system by their own. This project is focusing on developing a house security system with an active infrared motion detector, pressure sensor, magnetic sensor and light sensor which are controlled using FPGA programmed by VHDL language. The overall project is divided into two parts. The first part is concern on the hardware development. The second part is based on software programming to operate the hardware structure. As the result, sensor is capable to detect motion while the programmed. FPGA is capable to control the whole operation of the security system.

KEYWORDS: FPGA, VHDL, StateCAD, Digilent adept, Xilinx ISE, RLT, Schematics

I. INTRODUCTION

Automation is the use of scientific and technological principles in the manufacture of machines that take over work normally done by humans. The manual security provided to the property of individuals or industries is costlier

Human errors may affect the whole security drastically and single mistake may fail the whole purpose. Hence automation in the security purpose is necessary. There are some high quality security systems already available in the market.

In addition to this, many homeowners may not feel the need to actually invest in a professionally installed security system. Many individuals who rent their homes,

Such as apartment owners, are usually not allowed to install permanent devices in their homes. Also most inexpensive home security devices and components are nothing more than cheap and ineffective noise makers.

We desired to innovate a security system assembled using VLSI technology that would be:

- AFFORDABLE in order to appeal to the general public.
- RELIABLE in order to operate without failure.
- EFFECTIVE in order to provide a sense of security.

This report presents an investigation and implementation of security system based on VLSI technology. Advantages of VLSI-FPGA based project are smaller size, lower cost, lower power, higher reliability, more functionality. There are now two industry standard hardware description languages, VHDL (Very high speed integrated circuit Hardware Description Language) and Verilog. The complexity of FPGA designs has meant an increase in the number of specialist design consultants with specific tools and with

their own libraries of macro and mega cells written in either VHDL or Verilog. So the objective of minimizing human efforts is going towards completion.

II. TOOLS USED

A. StateCAD:

StateCAD is a graphical entry tool that allows engineers to express their ideas in a natural manner, as state diagrams. This allows for designs without cumbersome, text oriented and error prone rules.

B. Xilinx ISE:

Xilinx Tools is a suite of software tools used for the design of digital circuits implemented using Xilinx Field Programmable Gate Array (FPGA) or Complex Programmable Logic Device (CPLD). The design procedure consists of (a) design entry, (b) synthesis and implementation of the design, (c) functional simulation and (d) testing and verification. Digital designs can be entered in various ways using the above CAD tools:using a schematic entry tool, using a hardware description language (HDL) – Verilog or VHDL or a combination of both. In this lab we will only use the design flow that involves the use of Verilog HDL.

C. Xilinx Spartan-3E FPGAs:

spartan-3E Low-Cost Features the Spartan-3E family reduces system cost by offering the lowest cost-per-logic of any FPGA family. Supporting the lowest-cost configuration solutions including commodity serial (SPI) and parallel flash memories, and efficiently integrating the functions of many chips into a single FPGA .

D. Digilent Adept 2:

Adept™ is a suite of Windows-based applications that can transfer programming files and other data between a PC and Digilent boards. Adept typically uses a USB2 port for communications, but Ethernet, Serial, and Parallel ports are also supported

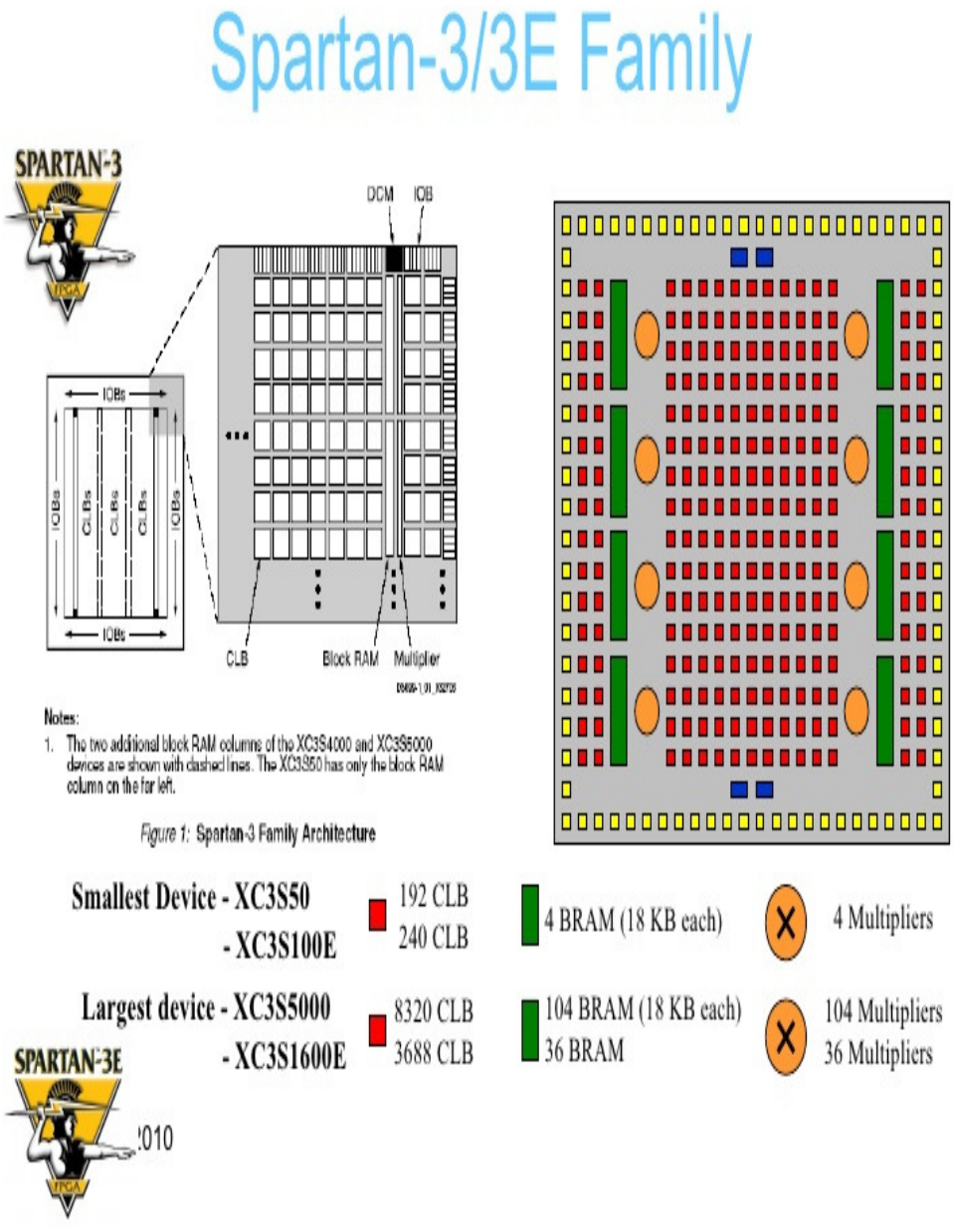
III. CURRENT WORK DONE

Objectives: Generate Finite state machine (FSM) or finite state automaton design of a digital security alarm using StateCAD, and implementation on a Digilent FPGA Spartan 3 Starter kit board.in part I we will generate the VHDL code. StateCAD allows visual implementation of a State Diagram and translation into a Hardware Description Language(HDL) code. It is not necessary to understand the HDL code, however we have little control over how the software translates the state diagram.
We will create a state diagram for a car security alarm, and generate VHDL. In part II we will simulate our state diagram to check whether it behaves like we expect. In part III we will create the schematic symbol and implement the VHDL code in our Diglent Spartan 3 board, and finally test the digital security alarm to ensure that it works as expected.

Overview: FPGA (Field Programmable Gate Array) is a chip containing a matrix of logic cells with programmable interconnects, which can be configured by a user. By configuring the function of each logic cell and the way they are connected between each other, one can make FPGA implement any digital circuit (limited only by the capacity of the device).
FPGA provide the next generation in the programmable logic devices. The word Field in the name refers to the ability of the gate arrays to be programmed for a specific function by the user instead of by the

manufacturer of the device. The word Array is used to indicate a series of columns and rows of gates that can be programmed by the end user.

FPGA devices are customized by loading configuration data into internal memory cells. The FPGA device can either actively read its configuration data out of an external serial or byte-wide parallel PROM (master modes), or the configuration data can be written to the FPGA devices (slave and peripheral modes).



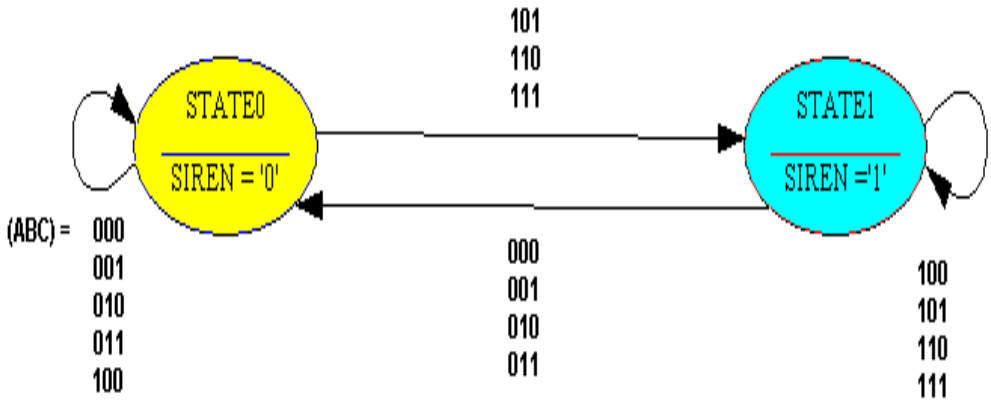
A complete workflow of an FPGA design is normally:

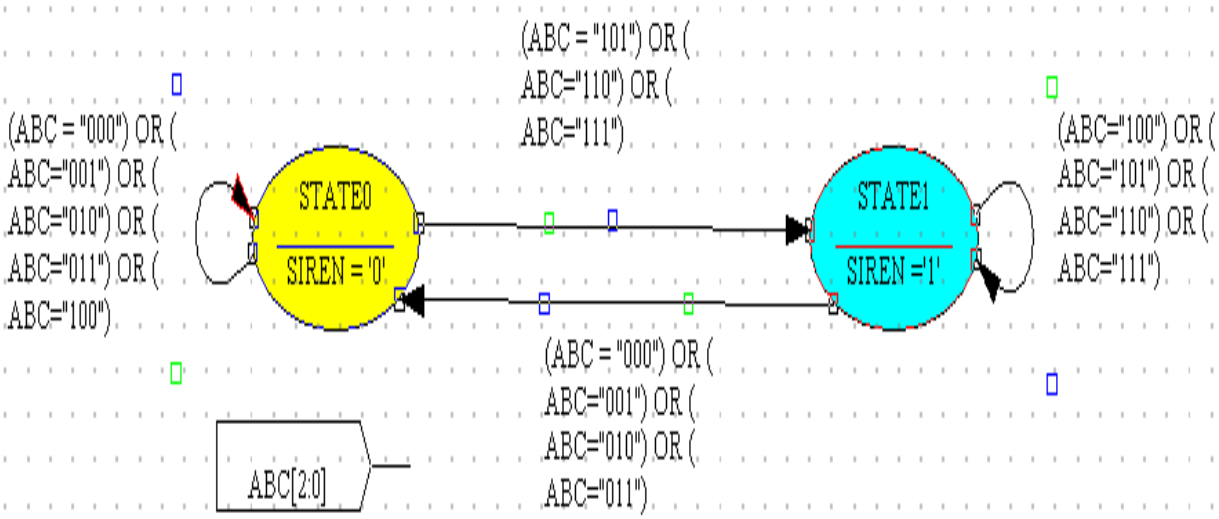
- Problem/requirements analysis, vendor selection
- Behavioral model design
- RTL (Verilog or VHDL) design
- RTL verification
- Logic synthesis
- Implementation
- Static timing analysis

IV. DIGITAL SECURITY ALARM SPECIFICATIONS

We will devise a Digital Home Security Alarm that will sound a siren if the alarm system has been energized i.e. armed (A=1) and the door is open (B=1) and / or an ultrasonic sensor signals movement inside the home (C=0).

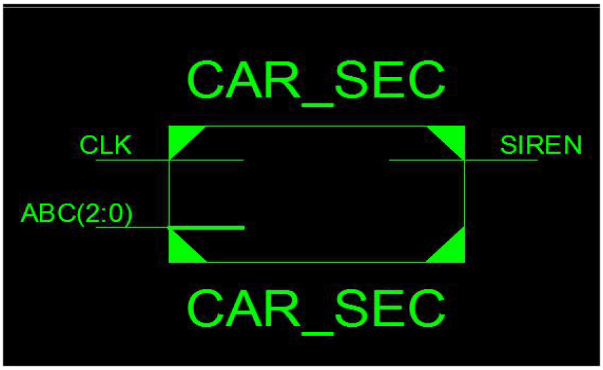
We need to ensure that when the door has been opened in an unauthorized manner, or a presence is detected by the ultrasonic sensor within the home, the alarm siren will sound. This is achieved with a Finite State Machine (FSM) as shown:



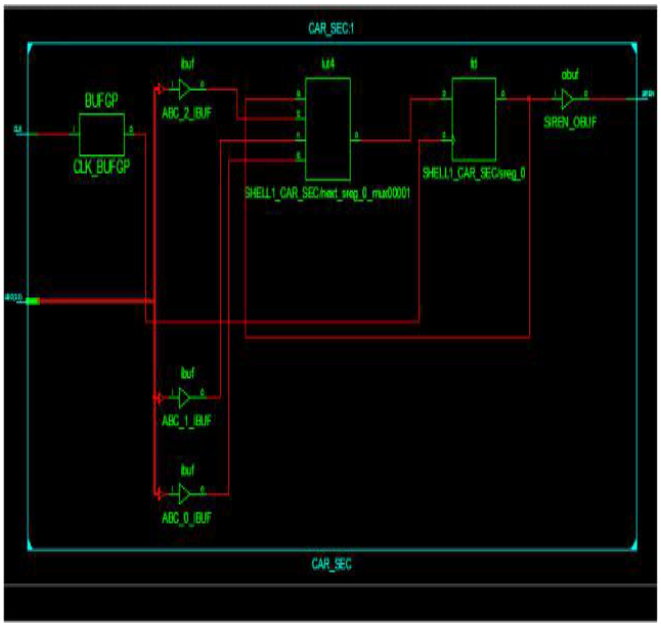


1) In STATE0 the siren is off (SIREN=0) if the alarm is not energized that is armed (A=0) and the door (B) or the ultrasonic sensor (C) can be in any combination, or if alarm is armed (A=1) the siren will not sound if door is closed (B=0) or no presence is detected within the home by the ultra sonic sensor (C=0).
2) There is a transition from STATE0 to STATE1. if alarm is armed (A=1) and if either the door is open (B=1) or ultrasonic sensor detects a presence within the home (C=1) or both the door is open and ultrasonic sensor detects (B=1 and C=1), the siren will sound, and the system will remain in STATE1.
3) The system will remain in STATE1 that is. siren will be sounding whatever happens next to the door (either is closed or open or sensor detects or not, provided the alarm is still armed (A=1).
4) Transition from STATE1 to STATE0 occurs only if the system is disarmed (A=0). And in this circumstance for B or C, the siren will not sound anymore (SIREN=0).
We have designed a State Diagram in StateCAD and compiled a VHDL file.
In part II we will simulate the state diagram and in part III we will program our Digilent Spartan 3 board, and test physically the logic circuit.
In part I we have generated VHDL code from a State Diagram. We will now simulate the state diagram in order to debug it, and to ensure that it behaves as expected.
With StateBench we can go through our design one clock cycle at a time, changing inputs and verifying outputs.

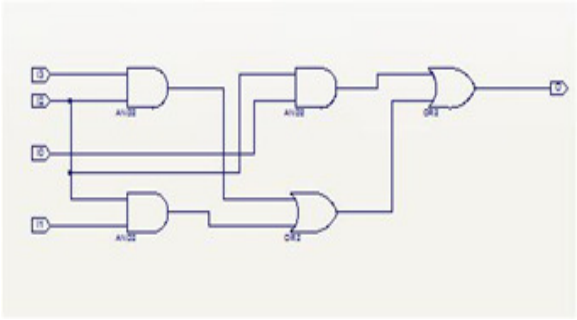
The Main Schematic:



If we click the block diagram, we will see:



By clicking LUT4 block we will see the logic circuit:



V. RESULTS

The alarm security circuit will light up a LED (LD0) on Spartan 3 Starter kit board, simulating SIREN sounding, only when the conditions we have established of state machine occurs.

On Digilent Spartan 3 board, the leftmost switch represents ALARM armed or unarmed (upward or downward respectively) the rightmost switches are DOOR (upward door open, downward door closed) and ULTRASONICSENSOR (upward presence detected and downward no presence).

VI. CONCLUSION AND FUTURE SCOPE

We first designed the State Diagram in StateCAD and generated VHDL, Then we simulated our state diagram in StateCAD to verify whether it behaves as expected. We imported the VHDL file of part I in Xilinx ISE Project Navigator, and we followed all the procedures to implement our VHDL in an FPGA. We have successfully programmed the Digilent Spartan 3 Starter kit board, and tested our digital home Security Alarm state machine we designed in part I.

This VLSI system is further modified for the many applications. It can be used in office for automatic door close system.
It can also be used in automatic door lock system in houses, cars and offices after fixed time slot or fix duration.
It can be used in remote interface which give a more reliable program.
It is also use in industry in many applications. By adding video camera (for cost effective purpose), this system can be used as low cost home security system for apartments.

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